

AMENDMENTS IN THE SPECIFICATION

Please replace paragraph [0025] with the following:

As depicted in Figure 4, the self-test system 48 includes a random digital sequence generator 52 which issues a series of digital "1" and "0" bits in a random sequence. A suitable random digital sequence generator 52, for example, takes the form of a linear feedback shift register to generate the random sequence of digital bits. The random output sequence of digital bits from the generator 52 is furnished to an activate circuit 54. ~~In one embodiment, the random digital sequence generator 52 and the activate circuit 54 are included within a single component, referred to as the activator 51.~~ As will be set forth, the activate circuit 54 includes a time adjust system 56 (Figure 5) which, on receipt of signals on line 50 introduces time delay or jitter in the data windows. At such times, the activate circuit 54 sends test data in the form of the random digital sequence from generator 52, but in data windows or eyes which are delayed in the opening or advanced in their closing, or both, like the data windows 14 of Figure 2.

Please replace paragraph [0035] with the following:

Figure 5 in the drawings depicts a preferred embodiment of the activate circuit 54. The incoming stream of bits, whether SYSTEM DATA or a random series of bits from the random sequence generator 52, is fed to each of a pair of latches 63 and 65. The latches 63 and 65 are set to operate and store alternating bits, "ODD" and "EVEN", in the sequence of bits received from the generator 52. Latch 63 is termed an even bit latch and latch 65 is termed an odd bit latch. The latches 63 and 65 are connected to a multiplexer [[66]] 67 where the alternating bits are recombined. Thus, either SYSTEM DATA or serial test data in the recombined form of the original random bit sequence from the generator 52, is presented to the multiplexer 60. The multiplexer 60 allows the bit sequence to pass to an amplifier of driver 62 and to an amplifier in driver 64.

Please replace paragraph [0039] with the following:

The time adjust system 56 further receives the serial data from the multiplexer [[66]] 67 at a delay block circuit 86 which introduces a delay δ . The delay δ is set to be $\frac{1}{4}$ of a bit period. The output of delay circuit 86 is furnished to a delay circuit 88, which includes a delay γ which is

set to be $\frac{1}{4}$ of a bit period, and to each of a pair of logic functions **90** and **92**. The output of delay circuit **88** is furnished to a delay circuit **94** which includes a delay γ which is set to be $\frac{1}{4}$ of a bit period. The output of delay circuit **88** is also sent to logic functions **90** and **92**, and to a third logic function or gate **96**. The delay circuit **94** is sent as an input to the logic functions **90** and **92**.